DESIGN GUIDE FOR ELECTROMAGNETIC DELAY LINES

PCA ELECTRONICS, INC.

DELAY LINE CATALOGUE

PCA ELECTRONICS has supplied transformers and networks to industry since 1951. Our pulse transformers, delay lines, special purpose filters and equalizers are used in many of the military space and commercial systems. An elaborate manufacturing facility together with the most progressive test equipment available to the industry and a team of skilled engineering specialists have functioned to keep PCA leadership in the space age.

This catalog is an attempt to help the circuit designer select and specify the delay line that will best suit his needs. Since the varieties of delay lines that can and have been built are almost infinite in number, we will explain the characteristics, electrical and physical properties of delay lines in general and let the designer "do it himself" rather than list a group of lines already designed and hope that one would meet his requirements.

The information contained in the graphs and charts is not intended to be restrictive; that is, lines with characteristics other than indicated are obtainable (higher voltages, lower impedances, longer delays, etc.) but space restrictions permit listing the characteristics of only the most popular type of lines. We will be most happy to help design lines for any of your requirements, standard or special.

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SECTION 1

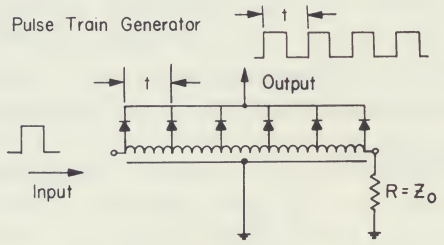
WHERE CAN I USE ELECTROMAGNETIC DELAY LINES?

Electromagnetic Delay Lines are merely a "compressed" form of a conventional transmission line and exhibit the same general electrical properties. The many advantages and innumerable uses of such lines have been a tremendous boon to the electronic industry for some of the reasons given below:

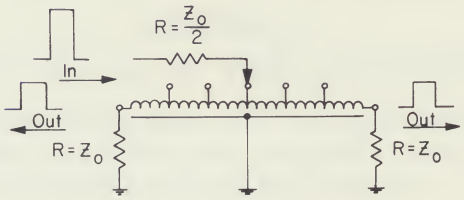
1. Useful frequency range from DC to 150 megacycles (admittedly the delays at the upper frequency range are in the order of nanoseconds).
2. Delay capabilities from nanoseconds to milliseconds.
3. Ability to temporarily store many "bits" of information using pulses.
4. Low-Loss Passive devices that require no power (other than the input signal) and which are very stable with time and temperature.
5. Useful as energy storage devices.
6. Constant delay for sine wave signals over the useful frequency range of the line.
7. Versatility and ease of design allow "custom Transmission lines" to fit your electrical and package requirements.

Since a transmission or delay line can reflect energy from the termination back to the signal source if the line is terminated in anything other than a resistance equal to Z_0, the designer may employ an infinite number of combinations of line impedances, input pulse widths, and repetition rates, taps, line terminations, source impedances, input polarities and circuit configurations to yield almost any pulse behaviour pattern that he desires; a few basic examples are illustrated below.

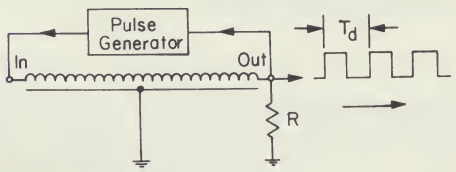
Pulse Train Generator



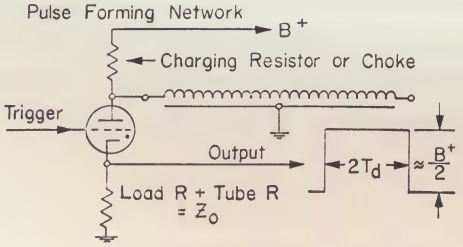
Step Variable Line With Low Impedance Output



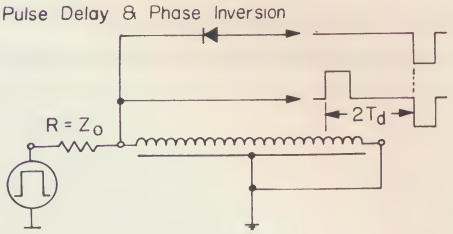
Clock (Output Pulse Generates New Input Pulse)



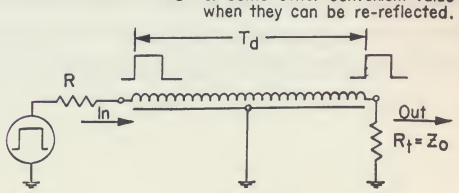
Pulse Forming Network



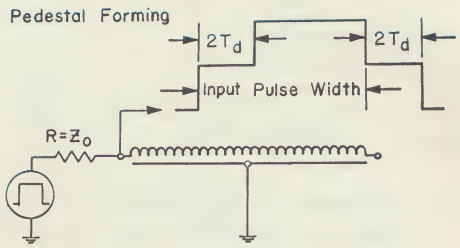
Pulse Delay & Phase Inversion



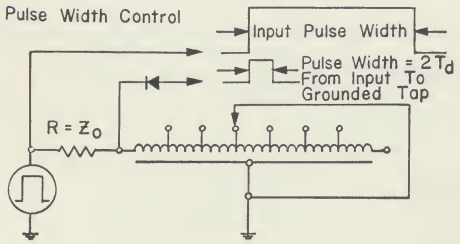
Straight Delay – $R = Z_0$ when reflections from output cannot be re-reflected.
$R = 0$ or some other convenient value when they can be re-reflected.



Pedestal Forming

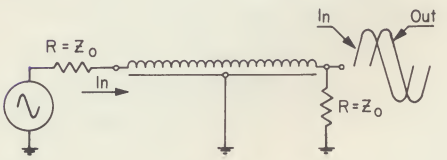


Pulse Width Control

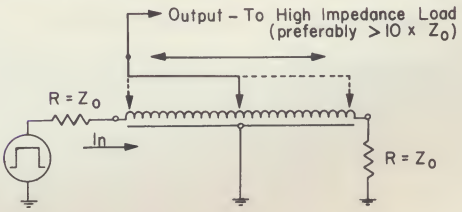


PHASE SHIFTING

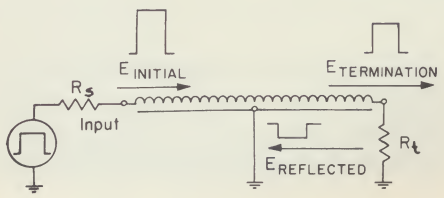
Phase Shift In Degrees = T_d(usec.) x f(mc.) x 360



CONTINUOSLY VARIABLE DELAY



As may be seen in the above examples, a line terminated in a short circuit returns all the energy to the line (neglecting line attenuation) with the reflected voltage of the opposite polarity (180° phase shift) from the original signal. An open circuited line also returns all the energy, but the reflected polarity is the same as that of the original signal. If the designer wishes to return only a part of the energy, formulas to determine the termination and reflected voltage in terms of the relationship between the terminating resistance and Z_0 of the line are given below:



$$E_{\text{Termination}} = \frac{E\ \text{Initial}}{\frac{Z_0}{2R_t} + \frac{1}{2}}$$

$$E_{\text{Reflected}} = E_{\text{Initial}} \left\{ \frac{1}{\frac{Z_0}{2R_t} + \frac{1}{2}} - 1 \right\}$$

EXAMPLE: Assume an input pulse of 1 volt to a line with a Z_0 of 1000 ohms which is terminated in 500 ohms.

$$E_{\text{Termination}} = \frac{1}{\frac{1000}{2 \times 500} + \frac{1}{2}} = \frac{1}{1.5} = .667 \text{ volts}$$

$$E_{\text{Reflected}} = 1 \left\{ \frac{1}{\frac{1000}{2 \times 500} + \frac{1}{2}} - 1 \right\}$$

$$= \frac{1}{1.5} - 1 = -.333 \text{ volts}$$

These formulas do not include the effects of line attenuation.

The voltage gain or loss at the termination expressed in db as a result of a mismatch at the termination is

$$db = 8.6858 \log_\epsilon \frac{1}{\frac{Z_0}{2R_t} + \frac{1}{2}}$$

Example:

What would be the worst-case condition of a voltage loss at the output if the Z_0 is at the high limit of its $\pm 10\%$ tolerance and the terminating resistor is at the low limit of its $\pm 5\%$ tolerance?

$$db = 8.6858 \log_\epsilon \frac{1}{\frac{1.1}{2 \times .95} + \frac{1}{2}} = 8.6858 \log_\epsilon .928$$

$$= 8.6858\ (-.0748) = -.65 \text{ db}$$

SECTION 2.

WHICH SHALL I USE, DISTRIBUTED OR LUMPED CONSTANT?

Use **Distributed** when the following characteristics fit the application.

1. Delays < than 1 usec
2. td/tr ratios 12:1 or less
3. Attenuation allowance of 1 → 2 db/usec
4. Temperature Coefficients of ~200PPM/°C (2% delay changes for 100°C temperature change)
5. Low Distortion: 10% max; 5% typical
6. Small size, economy
7. Normal impedance ranges of 200→2000 ohms

See bulletin CDL 1159 and HDL 1159 for typical examples of distributed constant lines.

Use **lumped Constant** where any of the following characteristics are required.

1. Large Delays (> 1 usec)
2. Temperature coefficients of 50→100PPM/°C or better
3. Attenuations of 0.50 db/usec or less
4. td/tr ratios of > 12:1 required (ratios may exceed 100:1)
5. High voltages (> 1000 volts)
6. Extremely high or low impedances (5 ohms→30K ohms in special cases)

Both types are electromagnetic, but the distributed type derives its capacitance by the thickness and type of dielectric between the winding and a ground plane; the solenoid winding also generally does not use a magnetic core. The even "distribution" of inductance and capacity along the distributed type delay line accounts for its low distortion of the pulse shape.

The lumped constant type of line consists of many discrete "lumps" of capacity and inductance; magnetic cores are generally used and this allows low attenuation specifications.

The temperature coefficients of the cores and capacitors are low initially (generally 40 → 150 PPM/°C) and often can be partially cancelled by using cores with a positive coefficient and capacitors with a negative coefficient.

Both types may have taps placed at specified points along the line. There is no absolute limit to the number of taps that may be used or their proximity to each other; however, practical limitations of cost, available space for terminals and tap loading (see Section 5) all play a part in the choice of tap selection.

SECTION 3.

WHAT WILL BE MY TOTAL ATTENUATION?

The total voltage attenuation in an electromagnetic delay line is normally the cumulative effect of 5 separate possible sources of loss; they are —

1. The DC resistance of the line. The attenuation may be calculated in db $= \frac{4.35\ R}{Z_0}$ where R is the total resistance of the line and Z_0 is the characteristic impedance in ohms. The attenuation figures in Figure 2 are given for room temperature conditions; allow an increase in attenuation of 0.4% per °C for your expected temperature rise above ambient.
2. Dielectric and ground plane losses. For distributed constant lines, these losses may be as much as 25 to 50% of the DC resistance losses; for lumped constant lines they are negligible and may be ignored.
3. Loaded taps. See Section 5 to calculate this attenuation.
4. Mismatched termination. See Section 1 to calculate this attenuation if any possible mismatch is expected.
5. Pulse width limitation. This condition occurs when the input pulse width is less than 1.5 times the true rise time of the output pulse (measured using a wide input pulse). The sketch below shows the effect of a narrow input pulse upon the attenuation and pulse width of the output pulse. The effect on the output pulse width is known as "pulse stretching".

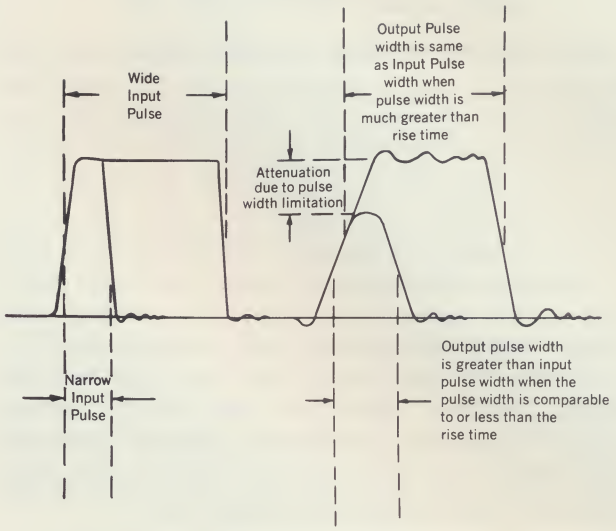
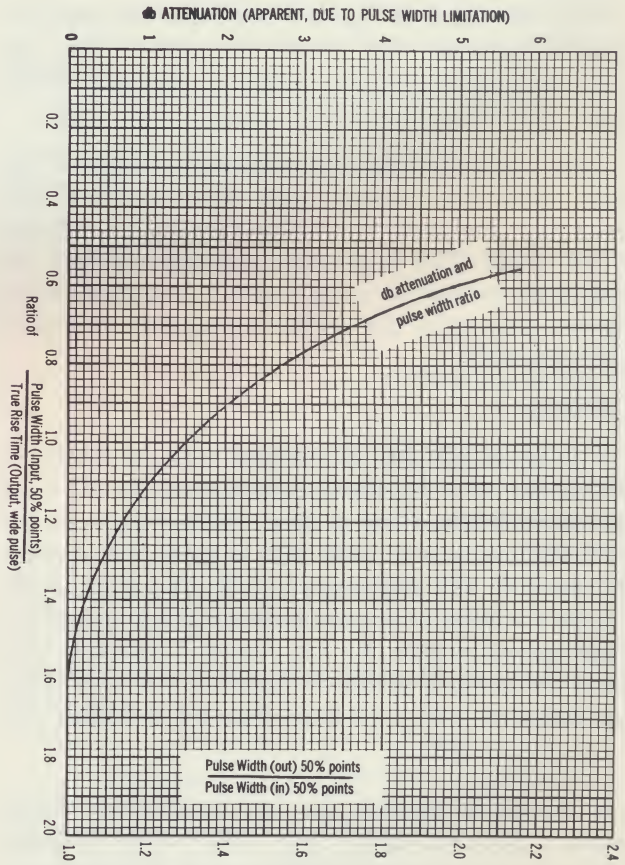


Figure 1 will give you the approximate value of attenuation in db and the ratio of output to input pulse widths when you know the input pulse width you will be using and the rise time that you specify for the output pulse. These figures are only approximate since they depend on the shape of the leading edge of the output pulse; this may vary from line to line.

FIGURE 1.



SECTION 4.

HOW SMALL CAN I MAKE IT?

Assuming that the delay has been determined by the application, and a lumped line will be used, the largest factor affecting size (and cost) will be the rise time and/or bandwidth required (see rear cover for relationship). Figure 2 graphically shows the approximate volume and weight of a delay line as a function of both the time delay to rise time ratio and the allowable attenuation. Caution should be exercised in the use of this chart; the weights and volumes shown are average and can easily vary by 25% or more depending upon the type of case material (plastic, aluminum, steel, etc.), potting material (epoxy, foam) efficient usage of case volume, number of taps specified, type of mounting specified (studs, inserts, wire leads) etc.

The charts also apply only under the following condition:

a. Dielectric strengths of 500 volts or less

b. Rise times between approximately .15 usec and 1 usec for the 4 solid curves.

Condition (b) is dictated by the permeability of the core material used; for rise times less than .15 usec double the attenuation shown on the curve being used; for rise times greater than 1 usec halve the attenuation shown.

The dotted line of Figure 2 indicates the performance the designer may require for lines in the 100 usec and greater category, although lines of either more or less attenuation may be quite easily built.

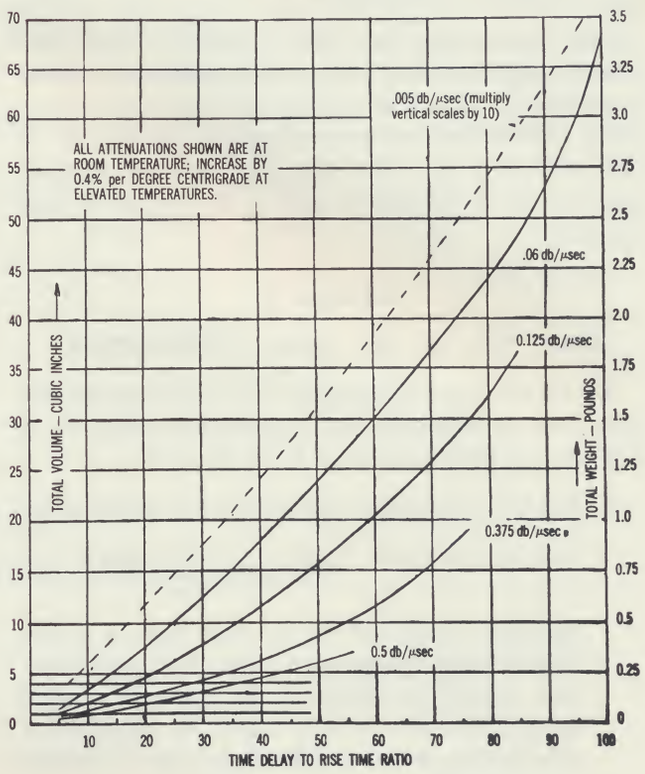
After one of the attenuation curves of Figure 2 has been tentatively selected, find whether or not the delay you have chosen will fit in the volume indicated by the graph. This is done by ascertaining first the time delay per section using Figure 3, and then checking this time delay per section calculation on Figure 4 for feasibility.

EXAMPLE:

A delay of 10 usec is required with an allowable attenuation of 2 db; the rise time must be .33 usec maximum. td/tr, then is 30:1. From Figure 2, the .125 db/usec curve looks like a good first choice. (10 usec X .125 db/usec = 1.25 db.) This would require a volume of approximately 8.2 in ^{3} and would weigh approximately .41 lbs. Figure 3 indicates that about 85 sections would be required; the time delay per section is $\frac{10}{85} \approx .12$ usec. Figure 4 indicates that this design is feasible for any impedance choice between 300 and 2000 ohms (500 ohms to 2000 ohms if a 500 working voltage rating is necessary).

If it looks as if your requirement may quite badly "stretch" one of the curves, please send us your tentative specifications and we will be more than happy to try and help you reach a satisfactory solution; perhaps by "giving" somewhat on a less critical parameter, we may be able to make a line that will meet your requirements.

FIGURE 2.



To determine which curve to use in figure 2, add up all losses except those due to the DC resistance of the line. (Attenuation shown in Fig. 2 is due to D.C. resistance only.)

Dielectric & Ground Plane Losses . . . . . db

Loaded Taps . . . . . db

Mismatched Termination . . . . . db

Pulse Width Limitation . . . . . db

Sub Total . . . . db

Then, the attenuation for use in Figure 2; (db) =

$$\frac{\left[\begin{array}{c}\text{total allowable} \\ \text{attenuation}\end{array}\right] - \left[\begin{array}{c}\text{sub total} \\ \text{above}\end{array}\right]}{[1 + .004 \triangle t\ (°C)]}$$

where $\triangle t$ is the expected rise in temperature above ambient.

FIGURE 3.

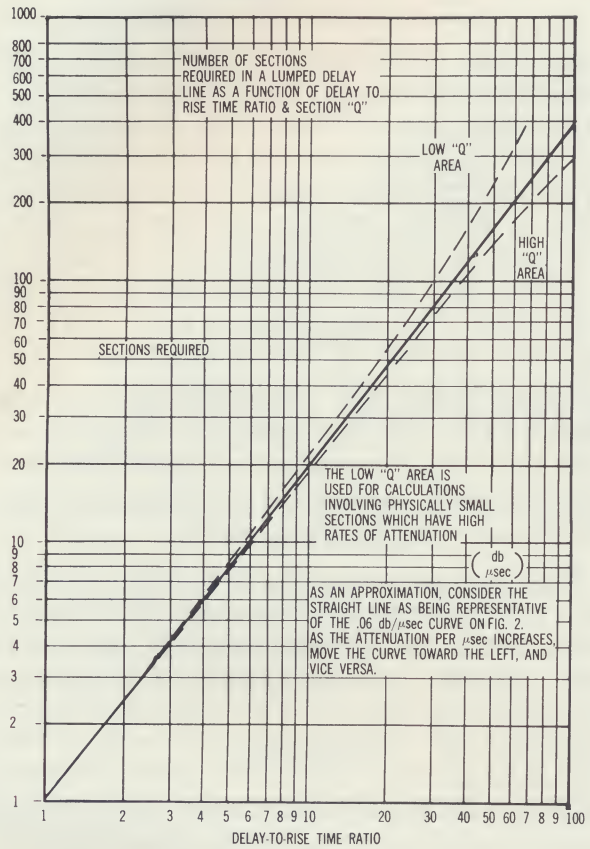
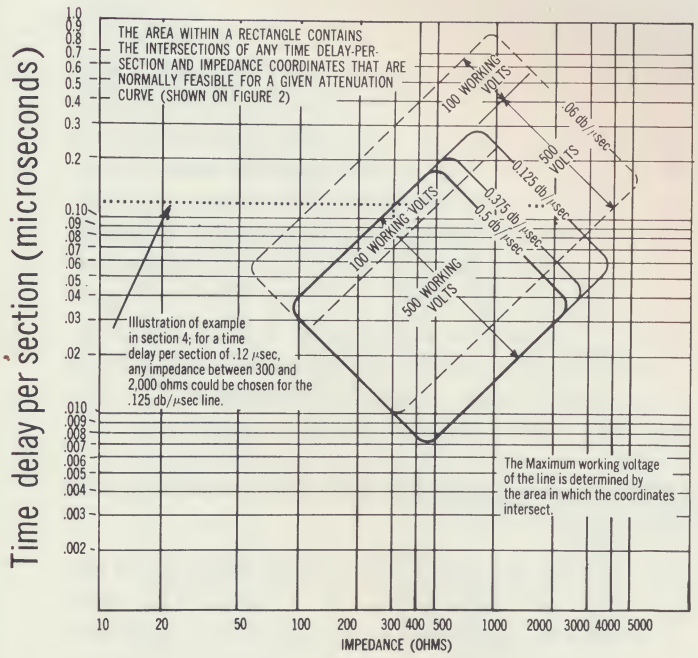


FIGURE 4.



SECTION 5.

WHAT ABOUT LOADED TAPS?

If delay line taps are loaded resistively, the pulse or signal will not be distorted, but some attenuation will occur; this attenuation may be calculated from

$$db = 8.6858\ \eta \log_\varepsilon \left\{ \frac{1}{1 + \frac{Z_0}{2R}} \right\}$$

Where η is the number of taps that are each loaded with R ohms; db will be the total voltage attenuation at the end of the line due to the tap loading. This is independent of the attenuation due to the DC resistance of the line. The two types of attenuation in db may be added directly to obtain the total attenuation.

It should be noted that a loaded tap will send energy back toward the source (negative polarity). This reflected voltage =

$$E\ \text{signal} \left\{ \frac{1}{1 + \frac{Z_0}{2R}} - 1 \right\}$$

and if large enough may cause distortion of a succeeding pulse at earlier taps or in the case of sine wave signals, will produce standing waves and delay variations.

EXAMPLE:

A line with a Z_0 of 470 ohms has 20 taps, each loaded with 15K ohms. The attenuation due to the loaded taps is

$$db = 8.6858 \times 20 \times \log_\varepsilon \left\{ \frac{1}{1 + \frac{470}{2 \times 15{,}000}} \right\}$$

$$= 173.7 \qquad \times \log_\varepsilon .98457$$
$$= 173.7 \qquad \times (-.0155) = -2.692\ \text{db}$$

If the attenuation due to the DC resistance of the line is 3.0 db, the total attenuation for the line is 2.69 + 3.0 = 5.69 db. In the event that the tap loads are not equal, set n = 1 and calculate the attenuation for each tap separately and then add the individual attenuations to obtain the total.

The reflected voltage from each tap in the example above is

$$E\ \text{Signal} \left\{ \frac{1}{1 + \frac{470}{2 \times 15{,}000}} - 1 \right\}$$

$$= E\ \text{Signal}\ (-.015)\ \text{volts}$$

Taps may sometimes have to be loaded capacitively, although this is to be avoided if at all possible. A tap may be loaded with as much as 5% of the per-section capacitance on a lumped constant line without introducing noticeable distortion but the delay at that tap and all succeeding taps will be increased. If you anticipate more than a few picofarads of capacitive loading, specify that the line be tested with that capacitance added externally. In cases where this loading is very high, the delay line manufacturer may be able to subtract this capacitance from the line capacitance if the taps are chosen to fall at a capacitor. Usually this means that the delay increments between taps must be an integral multiple of the time delay per section.

SECTION 6.

WHAT STABILITY AND ACCURACY OF DELAY CAN I SPECIFY?

In a large percentage of cases the temperature coefficient of delay can be designed to stay within ±50 PPM/°C on a lumped constant line without requiring testing of each line to assure conformity to this requirement. Lines can be built to tighter specifications, but at greater cost, since each line must be tested and individually corrected, if necessary.

Tolerances on delays at taps and the output can be held to a value equal to ½ the delay per section on lumped lines using normal production techniques; tighter tolerances can be held but at greater cost. In all cases the delay tolerance should be greater than 0.1 the rise time to avoid uncertainty of measurement. Distributed constant lines normally have a delay tolerance of ±5% or .01 usec, whichever is greater, although tighter tolerances can be held.

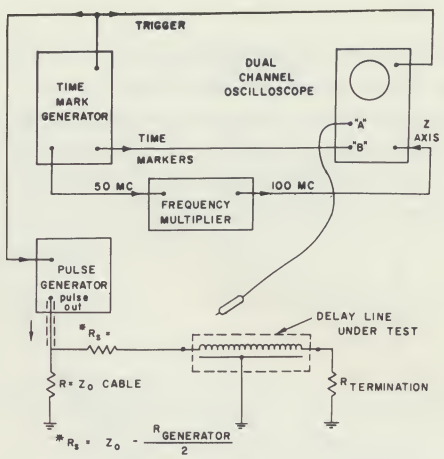
When selecting delay tolerances, compare the tolerance to be allowed at room temperature with the change expected over the temperature range; it is obviously uneconomical to hold close tolerances at room temperature if wide swings in delay are expected at the temperature extremes. Normally these two catagories of delay tolerance are comparable in value, however, it is quite often more economical to specify the total tolerance allowable with the understanding that it must hold over the entire temperature range; this allows the delay line manufacturer to select the most economical method of achieving the desired result.

SECTION 7.

HOW CAN I TEST THEM?

Delay lines for pulse circuitry may be measured in a test set up similar to the one shown below.

The choice of equipment is largely determined by the rise times and delay accuracies to be measured; for rise times greater than 20 nanoseconds and delay



tolerances larger than 5 nanoseconds, a Hewlett Packard 212 or 214 pulse generator with a Tektronix 180S time mark generator and a Tektronix 545 oscilloscope provide one suitable combination of many commercially available instruments.

When measuring rise times and delay tolerances down to the order of 1 or 2 nanoseconds, the oscilloscope usually used is of the "sampling" type and the pulse generator must be capable of generating a pulse with a rise time of 1.0 nanosecond or less at a reasonably high repetition rate (preferably > 1KC). A HP 215A generator with an HP 185B or a Tektronix 561A (with 3S76 and 3T77 plug-ins) oscilloscope are a suitable combination for these measurements. The "Z" axis intensity markers are not used with the sampling scope.

In general, use coaxial cable whenever possible to transmit the triggers, time marks, and pulses from one instrument to another. Terminate the cable carrying the output pulse from the generator in its characteristic impedance; the lead wires interconnecting the delay lines and source resistor and terminated cable should be as short as possible (generally less than 3" long) and should have very low capacitance to ground (less than 5 p.f.). Use a low capacity probe (from 0.5 to 12 p.f., depending on the line being measured) connecting the oscilloscope to the delay line. Extraneous lead length becomes of paramount importance as the impedance goes lower and the rise time gets smaller; a line with a rise time of 2 ns at an impedance of 50 ohms should not have leads longer than ⅛" if a reasonably accurate measurement of the delay lines' actual performance is to be obtained.

Basically, the method of time delay measurement is as follows:

1. Connect the probe to the input terminal of the delay line. Adjust the "A" channel gain such that the baseline of the pulse and graticule marking coincide and the average amplitude of the pulse top coincides with the top marking on the graticule. Be certain the input pulse voltage and rep. rate are as specified.

2. Reference a point on the leading edge of the input pulse (50% amplitude or a constant voltage, whichever is used) with one of the time marks on "B" channel.

3. Move the probe to the output, then using a sweep delay control built into the oscilloscope, delay the sweep until the output pulse is seen while counting the time marks that occur between the leading edges of the input and output pulse. 100 MC intensity markers on the Z axis of the oscilloscope allow easy subdivision of the basic time marks into .005 usec intervals. When measuring the delay at the output readjust the gain of "A" channel if the delay is being read at the 50% amplitude point to allow for attenuation between the input and output.

4. See EIA RS-242 for definitions of pulse parameters. This is obtainable from

   ELECTRONIC INDUSTRIES ASSOCIATION
   ENGINEERING DEPARTMENT
   11 West 42nd Street
   New York 36, New York

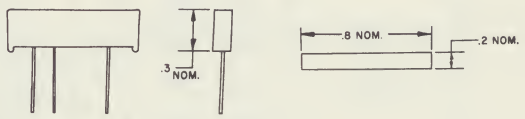
SECTION 8.

1. SPECIAL NOTES ON NANOSECOND LINES

The term "nanosecond" lines has come into general use to describe electromagnetic delay lines that have rise time less than 20 nanoseconds; the introduction and popular acceptance of the sampling oscilloscope has made it relatively easy to accurately measure lines with fast rise times and short delays.

Since the capacitance of a delay line $= \frac{\text{Time Delay}}{\text{Impedance}}$, the impedance of nanosecond lines should be kept low enough to avoid having the capacitance of the line be so small that problems are encountered with stray capacity. Generally, the impedance values of nanosecond lines range from 100 ohms to 1000 ohms. When the impedance becomes very low (50 → 100 ohms), care must be taken to keep lead lengths very short to reduce extraneous inductance to a minimum; lead lengths of 1/8" or 1/4" can be a problem if you are dealing with very fast rise times. If your choice of impedance is open, a value in the range of 200 → 500 ohms will generally avoid the two problems outlined above.

One advantage of the short delay of nanosecond lines is the very small volume requirement if your td/tr ratio requirement is not stringent. A delay of 20 to 60 nanoseconds may be put in a package volume of .05 → .08 in³ if a td/tr ratio of 3 to 1 is satisfactory. A typical case is shown below.



For the most part, both distributed constant and lumped constant nanosecond lines are packaged in plastic cases with wire leads on the bottom surface for printed circuit board mounting. The lines are usually small enough and light enough not to require any hold-down means other than the wire leads. Any lead breakout may be selected; bosses may be furnished on the bottom surface if requested. Modern molding methods allow low cost "special" cases even for small production orders.

TYPICAL DISTRIBUTED CONSTANT NANOSECOND LINES

DELAY (ns)	td/tr RATIO	MAXIMUM ATTENUATION (db)	Z_o ohms	CASE SIZE Width	Height	Length
25	9	1.0	50	1.04	.63	4.5
38	3.8	1.0	370	.33	.25	.9
50	4.1	1.0	316	.5	.5	1.53
75	4.7	1.0	316	.5	.6	2.0
125	7	1.0	1000	.437	dia	3.75
145	7.2	0.5	500	.5	.6	4.5

TYPICAL LUMPED CONSTANT NANOSECOND LINES

DELAY (ns)	td/tr RATIO	MAXIMUM ATTENUATION (db)	Z_o ohms	CASE SIZE Width	Height	Length
30	5	0.5	200	.5	.25	2.5
65	4.6	2.0	62	.34	.375	1.25
93	7.1	1.0	100	1.2	.275	1.1
300	15	0.5	200	1.0	0.7	3.0
420	21	0.5	500	1.04	.56	4.5

SECTION 8.

2. SPECIAL NOTES ON VARIABLE DELAY LINES

Delay lines which have the inductance constructed as a long solenoid with a sliding tap arranged to make contact anywhere along the winding provide a method of continuously varying the delay of a given signal. The resolution or smallest increment of delay adjustment is determined by the turn-to-turn delay; this varies depending on the physical length of the line, impedance, delay, etc. but typically is .001 times the total delay. The delay varies linearly with shaft rotation.

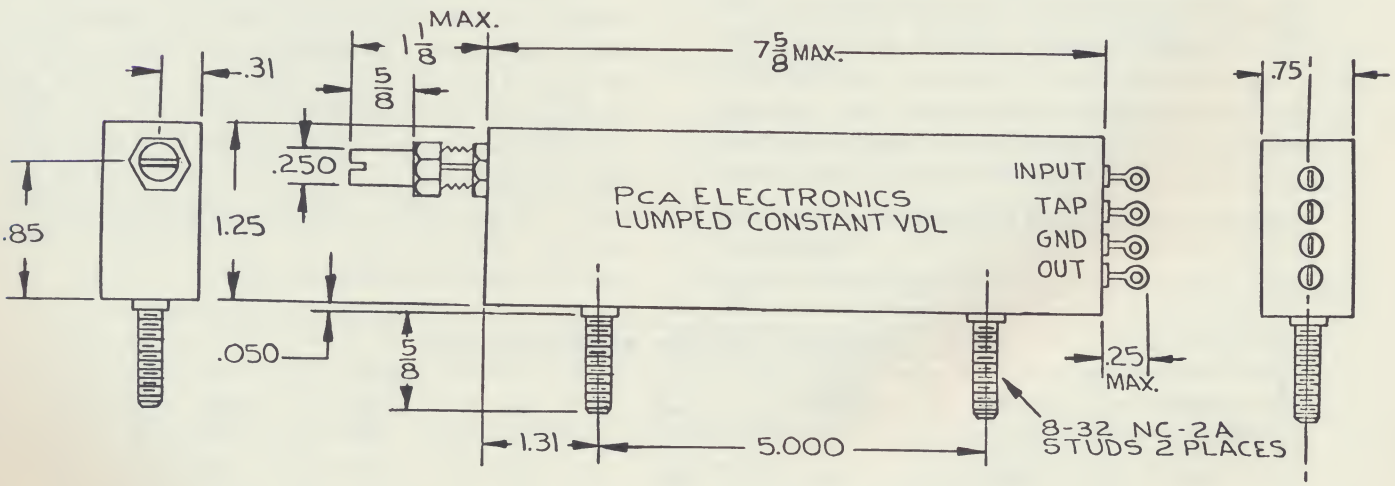
If the output of the line is taken from the sliding tap, the tap load should be at least 10 or 20 times the impedance of the line to prevent undesirable reflections (see Section 5).

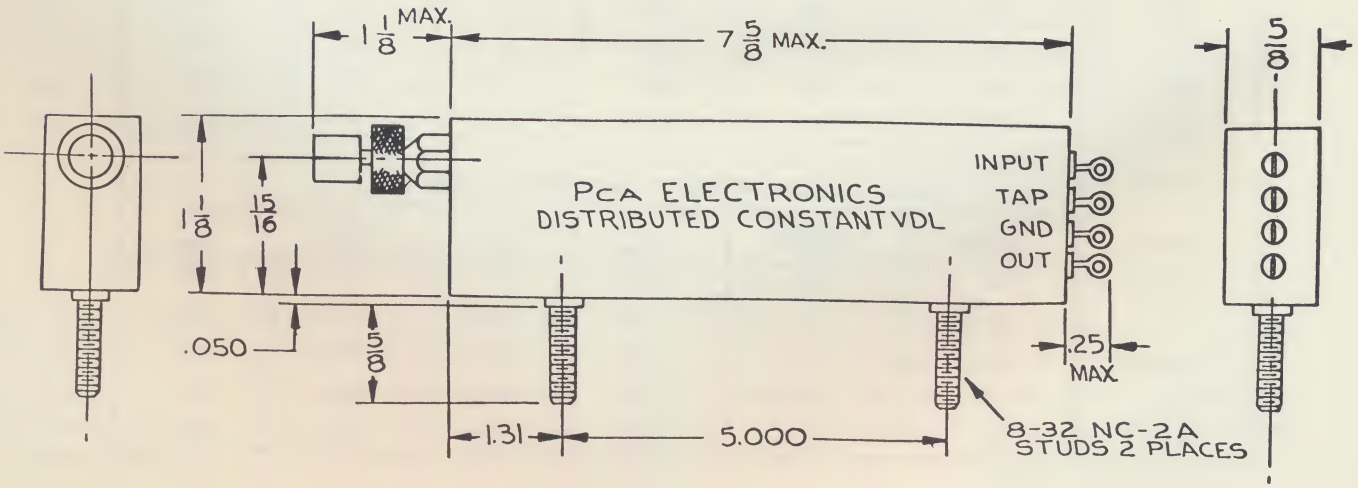
If a low impedance output is necessary, drive the delay line at the tap and terminate the line at both the "in" and "out" terminals with a load or resistance equal to Z_0. The useable output of the line then may be obtained at either the "in" or "out" terminal.

Variable lines may be built as either distributed or lumped constant types; characteristics of several standard designs which fit in the package illustrated below are as follows:

TYPICAL VARIABLE DELAY LINES

	PCA PART NO.	TIME DELAY (μSEC) +30% −0%	RISE TIME MAXIMUM (μS)	MIN DELAY RANGE	MAXIMUM ATTENUATION db	IMPEDANCE OHMS ±15%	DIELECTRIC STRENGTH
Distributed Constant	VDL 200 — 0.5	0.5	.06	5% to 95% of nominal delay	1.0	200	200 VDC 1K Megs "in" to "gnd." & all terminals to shaft
	VDL 1000 — 0.5	0.5	.06		1.5	1000	
	VDL 500 — 1.0	1.0	.125		2.0	500	
Lumped Constant	LVDL 1000 — 1.0	1.0	.11		1.0	1000	
	LVDL 250 — 2	2.0	.25		1.5	250	
	LVDL 125 — 4	4.0	.5		3.0	125	





GENERAL DELAY LINE FORMULAS

td = TIME DELAY
tr = RISE TIME (10% to 90% Points)

$$\text{RISE TIME (usec)} \sim \frac{.36}{\text{bandwidth (MC) at 3 Down Point}}$$

Assuming linear phase response of the line

Series Inductance

$L = td\ usec \times Z_0\ ohms$ (in microhenries)

Shunt Capacitance

$$C = \frac{td\ usec}{Z_0\ ohms}$$ (in microfarads)

L & C may be calculated for an individual section or a whole line

$$\text{ATTENUATION (db)} = \frac{4.35 \times R}{Z_0}$$

R is the DC resistance from the input to output terminal in ohms

$$Td\ usec = \sqrt{L_{uh} \times C_{uf}}$$

Time delay in microseconds

$$Z_0 = \sqrt{\frac{L_{uh}}{C_{uf}}}$$

= Characteristic impedance in ohms

Microsecond = 1×10^{-6} seconds

Nanosecond = 1×10^{-9} seconds

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